WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a memory cell portion on the semiconductor substrate in which a plurality of memory cells each having a charge storage layer are formed;

a peripheral circuit portion on the semiconductor substrate in which a circuit for controlling the memory cells is formed;

a plurality of active regions formed in each of the memory cell portion and the peripheral circuit portion and isolated from one another by a plurality of trenches;

insulating films with which the trenches are filled;

bird's beak-shape oxide films formed between the active regions and the charge storage layers of the memory cell portion; and

bird's beak-shape oxide films formed between the active regions and gate electrodes of the peripheral circuit portion, the bird's beak-shape oxide films being thicker than the bird's beak-shape oxide films formed between the active regions and the charge storage layers of the memory cell portion.

2. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a memory cell portion on the semiconductor substrate in which a plurality of memory cells each having a charge storage layer are formed;

a peripheral circuit portion on the semiconductor substrate in which a circuit for controlling the memory cells is formed;

a plurality of active regions formed in each of the memory cell portion and the peripheral circuit portion and isolated from one another by a plurality of trenches;

oxidation resisting films formed on inner walls of the trenches and side walls of the charge storage layers in the memory cell portion;

insulating films with which the trenches are filled;

gate insulating films formed between the active regions and the charge storage layers of the memory cell portion; and

gate insulating films formed between the active regions and gate electrodes of the peripheral circuit portion.

3. The nonvolatile semiconductor memory device according to claim 2, wherein the oxidation resisting films are silicon nitride films.

4. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a memory cell portion on the semiconductor substrate in which a plurality of memory cells each having a charge storage layer are formed;

a peripheral circuit portion on the semiconductor substrate in which a circuit for controlling the memory cells is formed;

a plurality of active regions formed in each of the memory cell portion and the peripheral circuit portion and isolated from one another by a plurality of trenches;

oxidation resisting films formed only on side walls of the trenches and only on side walls of the charge storage layers in the memory cell portion;

insulating films with which the trenches are filled;

gate insulating films formed between the active regions and the charge storage layers of the memory cell portion; and

gate insulating films formed between the active regions and gate electrodes of the peripheral circuit portion.

5. The nonvolatile semiconductor memory device according to claim 4, wherein the oxidation resisting films are silicon nitride films.

6. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a memory cell portion on the semiconductor substrate in which a plurality of memory cells each having a charge storage layer are formed;

a peripheral circuit portion on the semiconductor substrate in which a circuit for controlling the memory cells is formed;

a plurality of active regions formed in each of the memory cell portion and the peripheral circuit portion and isolated from one another by a plurality of trenches;

insulating films with which the trenches are filled; and

oxi-nitride films formed between the active regions and the charge storage layers of the memory cell portion; and

oxide films formed between the active regions and gate electrodes of the peripheral circuit portion.

7. A nonvolatile semiconductor memory device comprising:

a semiconductor substrate;

a memory cell portion on the semiconductor substrate in which a plurality of memory cells each having a charge storage layer are formed;

a peripheral circuit portion on the semiconductor substrate in which a circuit for controlling the memory cells is formed;

a plurality of active regions formed in each of the memory cell portion and the peripheral circuit portion and isolated from one another by a plurality of trenches;

oxidation resisting films formed on the inner walls of the trenches in the peripheral circuit portion;

insulating films with which the trenches are filled; and

gate insulating films formed between the active regions and the charge storage layers of the memory cell portion; and

gate insulating films formed between the active regions and gate electrodes of the peripheral circuit portion.

8. The nonvolatile semiconductor memory device according to claim 7, wherein the oxidation resisting films are oxi-nitride films.

9. The semiconductor memory device according to claim 7, further comprising oxidation resisting films formed on inner walls of the trenches and the side surfaces of the charge storage layers in the memory cell portion.

10. The nonvolatile semiconductor memory device according to claim 9, wherein the oxidation resisting films formed on inner walls of the trenches and the side surfaces of the charge storage layers in the

memory cell portion are oxi-nitride films.

11. A nonvolatile semiconductor memory device comprising: a memory cell array portion of a semiconductor substrate in which a plurality of memory cell transistors are formed in active regions of the semiconductor substrate and the active regions of the memory cell transistors oppose gate electrodes thereof and are insulated and isolated by an embedded device isolating regions; and

a peripheral transistor portion of the semiconductor substrate in which a plurality of peripheral transistors are formed in active regions of the semiconductor substrate and active regions of the peripheral transistors oppose gate electrodes thereof are insulated and isolated by an embedded device isolating regions,

wherein the curvature of device isolating ends of the active region of the peripheral transistor is larger than the curvature of the device isolating ends of the active region of the memory cell transistor.

12. The nonvolatile semiconductor memory device according to claim 11, wherein the difference between the height of a flat portion of the active region and the height of the lowest portion of the gate electrode upper than the flat portion is 4 nm or greater.

13. The nonvolatile semiconductor memory device according claim 11, wherein a bias potential with

which a sub-threshold current flows is applied to the peripheral transistor when the operation of the peripheral transistor is on standby.

14. The nonvolatile semiconductor memory device according to claim 11, wherein the gate electrodes of the memory cell transistors is self-aligned to the embedded device isolating region in the memory cell array portion.

15. The nonvolatile semiconductor memory device according to claim 11, wherein the memory cell transistor is a memory cell of a nonvolatile semiconductor memory including a charge storage layer.

16. A method of manufacturing a nonvolatile semiconductor memory device having constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a nonvolatile semiconductor memory device comprising the steps of:

forming a polycrystalline silicon layer on a silicon substrate through an insulating film;

providing a plurality of shallow trench isolation portions each having a bottom and formed to surround an active region for the silicon substrate by etching, in a self-aligned manner, the polysilicon layer, the insulating film and the silicon substrate in order to form an active region;

rounding edges at the device isolating side of opposite surfaces of the active region and the polysilicon layer by oxidation;

coating only the memory cell portion with a film having oxidation resistance; and

performing further-oxidation, after only the memory cell portion has been coated with a film having oxidation resistance, to provide a bird's beak-shape oxide film, the thickness of which is larger than the thickness of a bird's beak-shape oxide film in the memory cell portion, between ends of the opposite surfaces of the silicon substrate and the polysilicon layer.

17. The method of manufacturing a nonvolatile semiconductor memory device according to claim 16, wherein the oxidation resisting films are silicon nitride films.

18. The method of manufacturing a nonvolatile semiconductor memory device according to claim 16, wherein the oxidation resisting films with which the memory cell portion is coated are removed after the further-oxidation has been performed.

19. A method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell

portion, the method of manufacturing a nonvolatile semiconductor memory device comprising the steps of:

forming a polycrystalline silicon layer on a silicon substrate through an insulating film;

providing a plurality of shallow trench isolation portions each having a bottom and formed to surround an active region for the silicon substrate by etching, in a self-aligned manner, the polysilicon layer, the insulating film and the silicon substrate in order to form an active region;

rounding edges of opposite surfaces of the active region and the polysilicon layer by oxidation;

coating only the memory cell portion with a film having oxidation resistance;

selectively removing the oxidation resisting films so that the oxidation resisting films are left only on side walls of the charge storage layers and only on side walls of the trenches in the memory cell portion; and

performing further-oxidation, after the oxidation resisting films has been selectively removed, to provide a bird's beak-shape oxide film, the thickness of which is larger than the thickness of a bird's beak-shape oxide film in the memory cell portion, between ends of the opposite surfaces of the silicon substrate and the polysilicon layer.

20. The method of manufacturing a nonvolatile

semiconductor memory device according to claim 19, wherein the oxidation resisting films are silicon nitride films.

21. The method of manufacturing a nonvolatile semiconductor memory device according to claim 19, wherein the oxidation resisting films with which the memory cell portion is coated are removed after the further-oxidation has been performed.

22. A method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a semiconductor memory device comprising the steps of:

forming a polysilicon layer on a silicon substrate through an insulating film;

forming a first shallow trench isolation portion by, in a self-aligned manner, etching the polysilicon layer, the insulating film and the silicon substrate in only the peripheral circuit portion;

forming a bird's beak-shape oxide film by oxidizing edges of opposite surfaces of the active region and the first polysilicon layer in the peripheral circuit portion;

forming a second shallow trench isolation portion by, in a self-aligned manner, etching the polysilicon

layer, the insulating film and the silicon substrate in the memory cell portion; and

forming a bird's beak-shape oxide film, the thickness of which is smaller than the thickness of the bird's beak-shape oxide film formed in the peripheral circuit portion, by oxidizing ends of opposite surfaces of the active region and the polysilicon layer in the memory cell portion after the second shallow trench isolation portion has been formed.

23. A method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a nonvolatile semiconductor memory device comprising the steps of:

forming an oxidation resisting film on a silicon substrate through an insulating film;

selectively removing the oxidation resisting film and the insulating film in the memory cell portion;

forming a tunnel oxide film in the memory cell portion and nitrifying the tunnel oxide film to form the tunnel film into an oxi-nitride film;

forming a polysilicon layer on the tunnel oxi-nitride film in the memory cell portion and the oxidation resisting film in the peripheral circuit portion;

providing a shallow trench isolation portion for the memory cell portion and the peripheral circuit portion by, in a self-aligned manner, etching the polysilicon and the silicon substrate; and

providing a bird's beak-shape oxide film, the thickness of which is larger than the thickness of the memory cell portion, for the peripheral circuit portion by providing a bird's beak-shape oxide film for ends of opposite surfaces of the active region and the polysilicon layer by performing oxidation after the shallow trench isolation has been formed.

24. A method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a nonvolatile semiconductor memory device comprising the steps of:

forming a polysilicon layer on a silicon substrate through an insulating film;

forming a shallow trench isolation portion to form an active region by, in a self-aligned manner, etching the polysilicon layer and the silicon substrate;

rounding ends of opposite surfaces of the active region and the polysilicon by oxidation;

coating only the memory cell portion with a silicon film;

performing further-oxidation after coating with the silicon film has been performed to provide a bird's beak-shape oxide film, the thickness of which is larger than the thickness of the memory cell portion, for a space between ends of opposite surfaces of the silicon substrate and the polysilicon layer in the peripheral circuit portion; and

forming the silicon film covering the memory cell portion into an oxide film.

25. The method of manufacturing a nonvolatile semiconductor memory device according to claim 24, wherein the silicon film coated on the memory cell portion is an amorphous silicon film.

26. A method of manufacturing a nonvolatile semiconductor memory device having an active region constituted by a shallow trench isolation and including a memory cell portion having a charge storage layer and a peripheral circuit portion of the memory cell portion, the method of manufacturing a nonvolatile semiconductor memory device comprising the steps of:

forming a polysilicon layer serving as an insulating film and a charge storage layer for a silicon substrate;

forming a shallow trench isolation portions by etching the polysilicon layer and the silicon substrate in a self-aligned manner; and

forming a silicon oxi-nitride film on the inner

walls of the trenches and the side walls of the polysilicon layer.

27. The method of manufacturing a nonvolatile semiconductor memory device according to claim 26, wherein the process for forming the silicon oxi-nitride film on the inner walls of the trenches and the side wall of the polysilicon layer is a process for performing an oxide nitrifying process to form a silicon oxi-nitride film after the silicon oxide films have been formed on the inner walls of the trenches and the side walls of the polysilicon layer.

28. A method of manufacturing a semiconductor apparatus such that a portion of gate insulating film of MOS transistor is formed before formation of a device isolation and a remaining portion of the gate insulating film is formed after formation of the device isolation, the method of manufacturing a semiconductor apparatus comprising the step of:

forming an MOS transistor in such a manner that the curvature of ends of an active region of the MOS transistor having a gate insulating film which is formed after formation of the device isolation is larger than the curvature of the end of an active region of the MOS transistor having a gate insulating film which is formed before formation of the device isolation.

29. A method of manufacturing a semiconductor

apparatus such that a nonvolatile semiconductor memory is manufactured which includes a memory cell array region and a peripheral transistor region in which peripheral circuit transistors of the memory cell array region are formed, the method of manufacturing a semiconductor apparatus comprising the steps of:

forming a first gate insulating film for a memory cell transistor on the overall surface of a semiconductor substrate and forming a polysilicon film and an insulating film on the first gate insulating film;

providing trenches for forming device isolating regions for the insulating film, the polysilicon film, the first gate insulating film and the semiconductor substrate;

covering the memory cell array region and removing the first gate insulating film on ends of an active region of the peripheral transistor region;

oxidizing the surfaces of the trenches and surfaces between the ends of the active region of the peripheral transistor region and the polysilicon film on the ends;

embedding embedded insulators in the trenches to smooth the overall surface;

removing the insulating film on the polysilicon film;

removing the polysilicon film and the first gate

insulating film in the peripheral transistor region and forming a second gate insulating film for the peripheral circuit transistor;

forming, in the memory cell array region, a laminated gate structure having the polysilicon film as a charge storage layer and forming, in the peripheral transistor region, a gate electrode on the second gate insulating film; and

selectively introducing impurities serving as a source/drain of the transistor into the surface layer of the substrate.

30. A method of manufacturing a semiconductor apparatus such that a nonvolatile semiconductor memory is manufactured which includes a memory cell array region and a peripheral transistor region in which peripheral circuit transistors of the memory cell array region are formed, the method of manufacturing a semiconductor apparatus comprising the steps of:

forming a first gate insulating film for a memory cell transistor on the overall surface of a semiconductor substrate and forming a polysilicon film on the first gate insulating film;

providing trenches for forming device isolating regions for the polysilicon film, the first gate insulating film and the semiconductor substrate;

embedding embedded insulators in the trenches to smooth the overall surface;

providing an inter-gate insulating film for insulating a charge storage layer and a control gate electrode of the memory cell transistor from each other for the overall surface of the substrate;

removing the inter-gate insulating film, the polysilicon film and the gate insulating film in the peripheral transistor region to expose the active region;

etching edges of ends of the exposed active region in the peripheral transistor to form a round shape;

providing a second gate insulating film for the peripheral circuit transistor in the peripheral transistor region;

providing a laminated gate structure including the polysilicon film as a charge storage layer for the memory cell array region and providing a gate electrode on the second gate insulating film for the peripheral transistor region; and

selectively introducing impurities serving as a source/drain of the transistor into the surface layer of the substrate.